NCN6001DEMO/D

Using the NCN6001 Smart Card Interface

Demo Board V1.1 User Manual

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APPLICATION NOTE

INTRODUCTION

The NCN6001 is a mixed integrated circuit designed to support the interface between the smart card and the micro controller. Although it does not handle the data protocol, the chip must comply with the electrical parameters defined by the ISO7816 and EMV international specifications. Leaving aside the level shift necessary to adapt the smart card to the micro controller, the part handles the safety functions required by the ISO specifications. In particular, the Power Down sequence is fully implemented in the silicon, avoiding any uncontrolled operation when the card is randomly extracted, or when the power supply drops below the minimum specified level. On top of that, extra built−in functions make the device flexible enough to control any type of banking operation: clock divider, clock operation mode and a SPI interface, supports both synchronous and asynchronous cards are among the most powerful features.

This application note describes the NCN6001 operation, the programming mode, and the details of the demo board designed to handle the interface.

The manual describes a possible application built around the NCN6001. We thank you for choosing an ON Semiconductor part, and we hope this guide will help you to run our demo board. Please use the NCN6001 data sheet as a reference source. For an up−to−date document please refer to the NCN6001 data sheet, document number NCN6001/D, available through the Literature Distribution Center or via our website at http://www.onsemi.com.

Demo Board Overview

The demo board comes fully assembled, ready to operate, on a 3.2 × 2.5 inches board. Included are all the functions needed to evaluate the NCN6001 integrated circuit. The evaluation system shall provide the constant supply voltage (DC 2.70 V to 5.5 V) to activate the interface. Among the electrical parameters, the power supply must be capable to yield 100 mA minimum continuous DC current to operate the demo board properly. Poor power supply generates random lost of transaction with the card and are difficult to fix. In the event of trouble with the transaction, double check the power supply line, particularly the ripple, as high and fast transients are present on this line during the DC/DC operation. Peak current up to 300 mA can be developed when the card operates at full speed. On the other hand, the power supply must be capable to yield the current necessary for any sub blocks built around the interface.

The software, embedded into the external MCU, includes the useful NCN6001 routines to set up all the programmable functions and to handle the EMV transactions.

The board, built on a dual side, metal through holes, printed circuit, includes the NCN6001 chip, with test points and required passive components (L1, C3, C8, C9). A Low current LED (I_f = 2 mA) is used to display the DC/DC status. Provisions are made to get an easy access to the key parameters during the evaluation of this integrated circuit. The top view is given in Figure 1.

Equipment List to Evaluate the Circuit

- DC Lab Power Supply (typical: 5 V/500 mA)
- Power Cable
- Asynchronous or Synchronous Type Smart Card
- Digital Voltmeter
- Four Channels (Bw > 200 MHz) Digital Oscilloscope
- Micro Controller with Appropriate Software

System Power Up

Make sure the power supply output voltage is within the 2.70 V to 5.50 V range (if a current limit circuit is present, set it at 500 mA). Connect the demo board to the micro controller by means of the 50 pins ribbon cable (maximum length = 50 cm). The Vbat LED/D1 shall turn ON.

Default Set Up After a Vbat Power ON, or RESET Action

When the board is powered up, the built−in functions of the NCN6001 set the default configuration as follow:

CARD VCC = 3 V
CARD DETECTION = Normally Open
CARD CLOCK divided by 1 and Running (see Note 1)
CARD POWER = OFF

NOTE 1: CRD_IO, CRD_RST and CRD_CLK pins stay Low, until the CRD_VCC card power voltage is turned on (see product data sheet).

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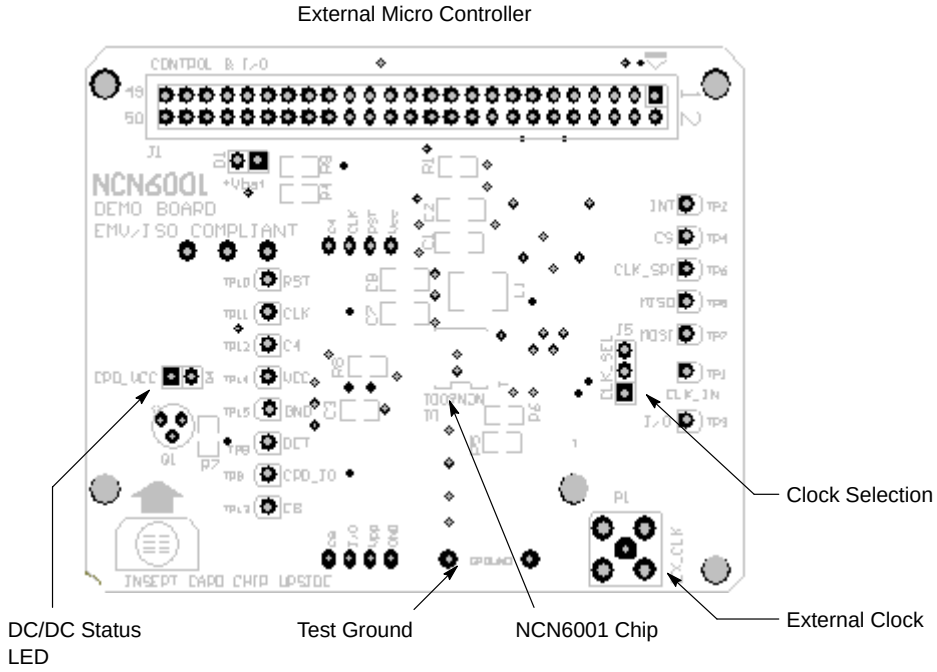


Figure 1. NCN6001 Demo Board Layout

NOTE 2: When the ON Semiconductor MCU motherboard is used, any action on the RESET push button forces the MCU to send this configuration to the NCN6001, avoiding any mismatch with the software saved in memory.

CARD POWER ON AND MEASUREMENTS

Connect the oscilloscope probes to CRD_RST, CRD_CLK, and CRD_IO. Use GROUND points as reference. Set up these three scope inputs at DC 5 V/div vertical scale and 100 μs time base.

Connect the fourth probe to low noise card CRD_VCC red test 14 point. A short ground connection is required. Set this channel at 1 V DC/div on your oscilloscope.

NOTE 3: When measuring ripple voltage, make sure to use a single Ground point for the four probes, or use the CRD_VCC probe only, the Ground being connected to test point 15.

To turn on the CRD_VCC voltage (thus, to run the internal DC/DC), the card detection switch must be activated (insert a smart card or a simulation tool). The card insertion yields an interrupt, the MPU acknowledges this signal and reads the STATUS bits, a command can be downloaded to activate the DC/DC converter.

NOTE 4: When no card is available during the NCN6001 evaluation, one can set up the CRD_DET as a Normally Close switch, making possible the DC/DC operation when no card is inserted (see CRD_DET specification). This engineering mode is possible since the demo board is built with a Normally Open switch mechanism, thus yielding a High level when no card is inserted. *However, such a mode must be avoided when a real card is inserted since the system will not operate when the mechanical switch is activated, thus forcing the CRD_DET pin to Low. In any doubt, reset the system and run a new set of measurements.*

The input clock (CLK_IN) can be derived from either the micro controller crystal (pre−wired mode), or connected to an external periodic signal, to generate the CRD_CLK . The selection is achieved by means of the JP5 CLK_SEL jumper according to Table 1 below.

Table 1. Clock Selection

Set CLK_SEL jumper to the TOP	→	Use the MCU clock (default position)
Set CLK_SEL jumper to the BOTTOM	→	Use the signal provided to the J5 SMA connector

When using an external signal, make sure to set up the external clock source to generate an appropriate peak−to−peak positive going signal, with appropriate frequency, making sure no overshoots/undershoots are developed at the clock input. The NCN6001 can accommodate 40 MHz input clock, but the clock divider must be adjusted to cope with the smart card (maximum ISO7816−3 operating clock is 20 MHz, EMV document specifies a 1 to 5 MHz range for banking applications).

Oscillograms

During the CRD_VCC rise time, all the smart card related logic lines are Low, avoiding the risk of uncontrolled data transaction with the card. When the voltage reaches the minimum programmed value, the lines are activated, according to the normative ISO7816−3 sequence, as

depicted in Figure 2. The logic levels present on these lines are the one defined by the micro controller and can be either 1's or 0's.

As depicted in Figure 2, approximately 300 mA DC current are absorbed from the power supply to charge the CRD_VCC 10 μF filter capacitor and to run the DC/DC converter. Failing to supply such a current will activate the Power Down Sequence if the CRD_VCC voltage does not reach the operating value within 4 ms.

Since no transaction can occur when CRD_VCC is below the minimum value, it is the engineer's responsibility to make sure the system is active prior to launch any smart card command. Such a check can be achieved by either reading the STATUS bit (preferred), or by forcing a 2 ms delay before to activate the card.

The power down sequence takes place when either a card is extracted, or when a fault is developed in the interface. In any case, the NCN6001 runs the ISO7816−3 normative sequence as recorded in Figure 3.

The three TOP traces in Figure 4 represent the CRD_VCC ripple as a function of the output voltage, the bottom trace represents the switching across the internal bridge structure.

Measuring the CRD_VCC ripple needs a lot of care to make sure the waveforms represent the right parameter. A couple of dedicated test points are provided on the NCN6001 demo board for such purpose: CRD_VCC and GROUND located TP14 and TP15. One single ground point must be used to carry out this test. As already depicted in the data sheet, using standard electrolytic or tantalum capacitor will downgrade the ripple, making the system more sensitive to EMV/ISO possible non qualification. The demo board comes with two X5R ceramic capacitors from Murata (C7 and C8) in parallel. However, a final product can be designed with either a single 10 μF or two 4.7 μF capacitors to save system cost, depending upon the PCB layout and wiring. A good technique is to split the CRD_VCC reservoir capacitor in two component, one being located as close as possible to the NCN6001 pins, the second being wired across the smart card ISO connector.

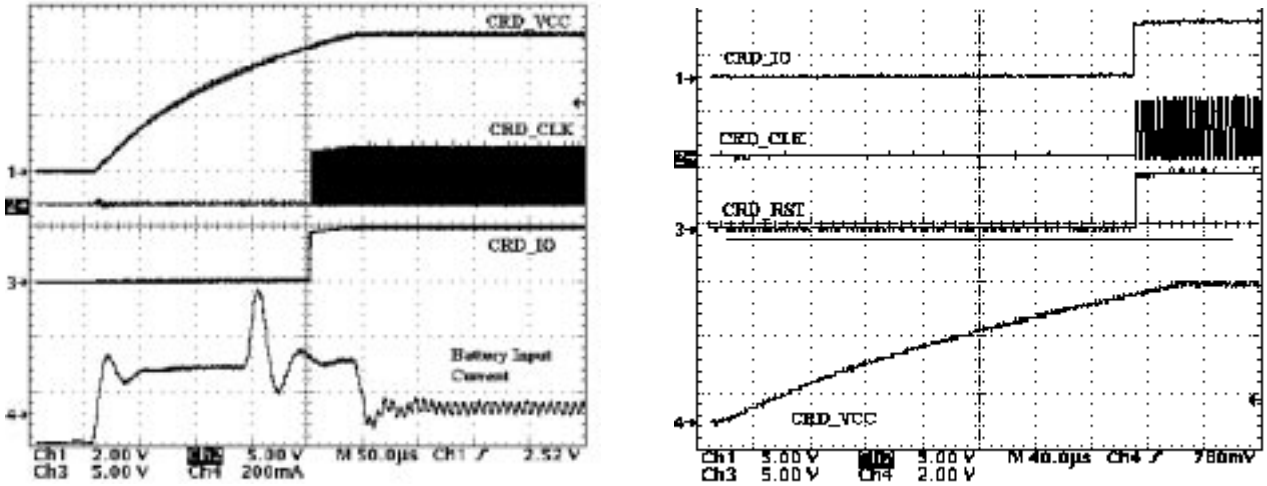


Figure 2. Power ON Sequence

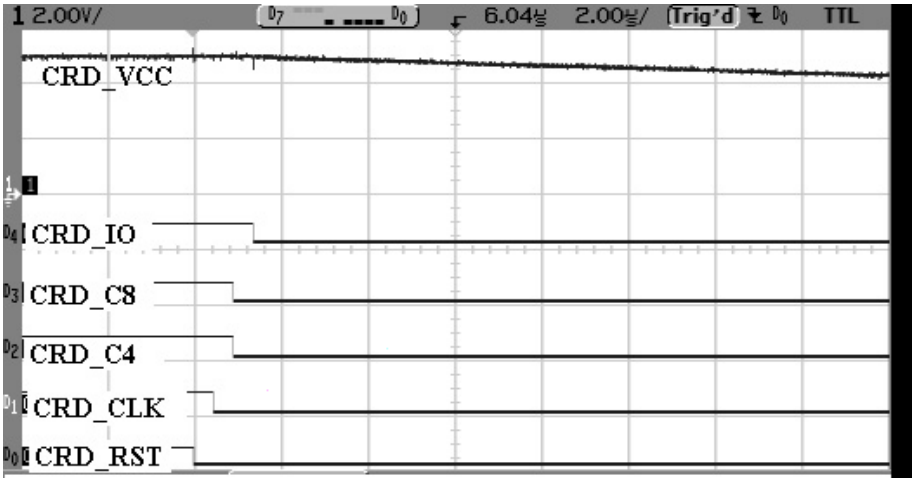
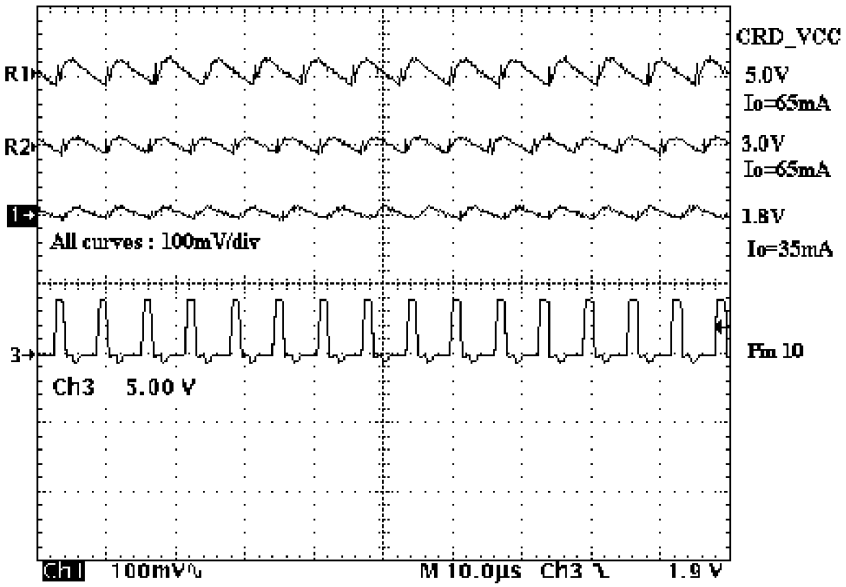


Figure 3. Power Down Sequence



Rload = 75 Ω, Vbat = 5 V, Cout = 10 µF, CRD_CLK = Running 1/1

Figure 4. CRD_VCC Voltage Ripple

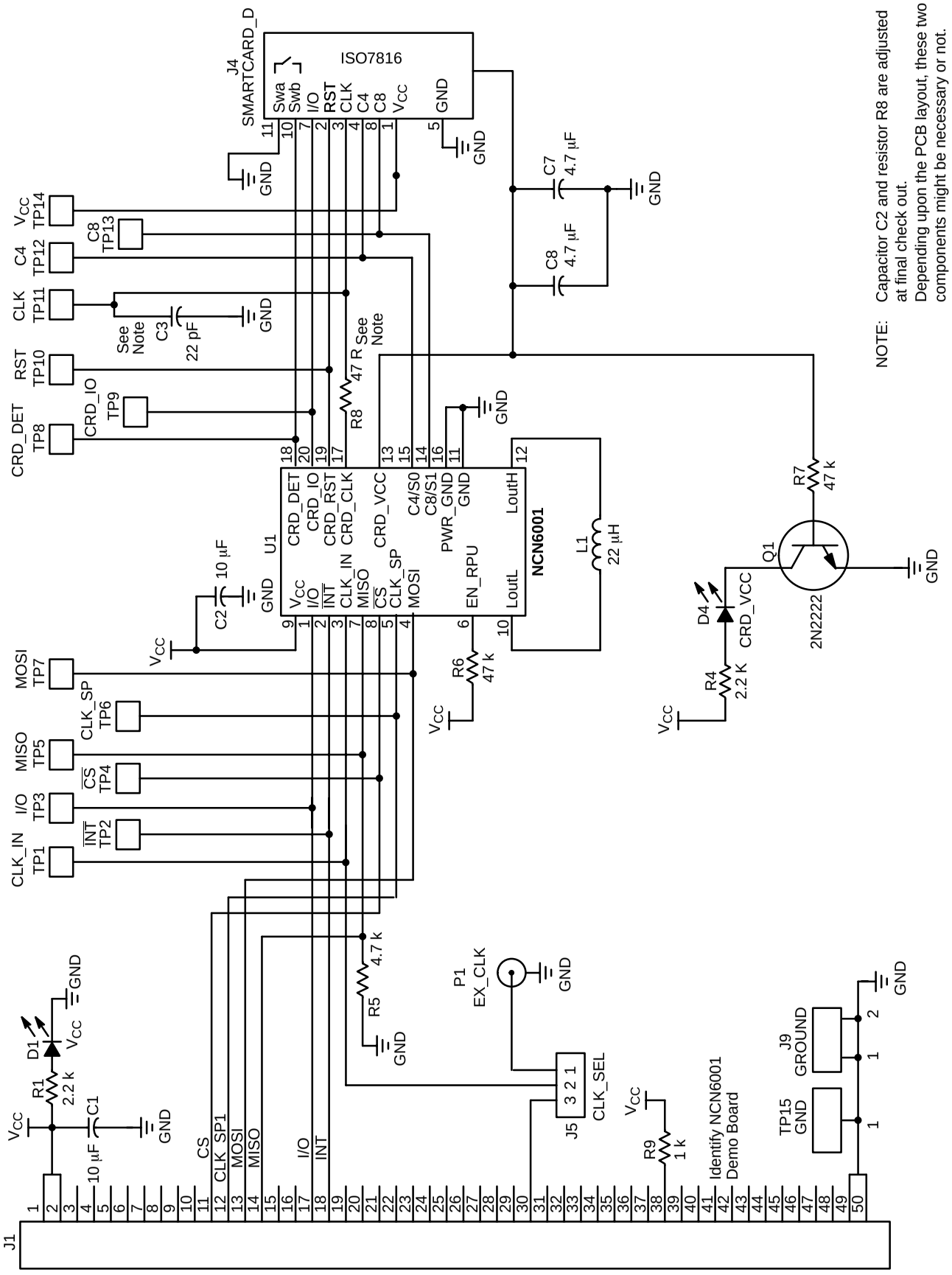


Figure 5. NCN6001 Main Schematic

Table 2. NCN6001 Demo Board V1.1 (B) Bill of Materials

Part	Designator	Footprint	Description	Preferred Suppliers	P/N
C1	10 μF/10 V	1206	Capacitor Y5V	MURATA	GRM42−6Y5V106Z10
C2	10 μF/10 V	1206	Capacitor X7R	MURATA	GRM42−6X7R106Z10
C3	22 pF*	805	Capacitor COG	MURATA	GRM40COG220J200
C7	4.7 μF/10 V	1206	Capacitor X5R	MURATA	GRM42−6X5R475K10
C8	4.7 μF/10 V	1206	Capacitor X5R	MURATA	GRM42−6X5R475K10
D1	Vbat	SIP2	LED diode green Round 3 mm I_F = 2 mA	Generic	−
D4	CRD_VCC	SIP2	LED diode red Round 3 mm I_F = 2 mA	Generic	−
L1	22 μH	1206	200 mA/1.2 Ohms	MURATA	−
J1	MCU	IDC50	50 pins ribbon connector	AMPS5−826629−0	−
J3	CLK_SEL	SIP3	−	−	−
J4	SMARTCARD_B	−	SMARTCARD_ISO	FCI	7434−L08−25S01
J9	GROUND	−	−	−	−
P1	EXT_CLK	SMA	−	Generic	−
R1	2.2 k	805	−	Generic	−
R4	2.2 k	805	−	Generic	−
R5	4.7 k	805	−	Generic	−
R6	47 k	805	−	Generic	−
R8	47 R*	805	−	Generic	−
R9	1.0 k	805	−	Generic	−
Q1	BC547	TO92L	−	ON Semiconductor	BC547B
U1	NCN6001	TSSOP20	−	ON Semiconductor	NCN6001/D
TP1	CLK_IN	TEST_PT	2.54 Red TEST_POINT	Generic	−
TP2	INT	TEST_PT	2.54 Red TEST_POINT	Generic	−
TP3	I/O	TEST_PT	2.54 Red TEST_POINT	Generic	−
TP4	CS	TEST_PT	2.54 Red TEST_POINT	Generic	−
TP5	MISO	TEST_PT	2.54 Red TEST_POINT	Generic	−
TP6	CLK_SPI	TEST_PT	2.54 Red TEST_POINT	Generic	−
TP7	MOSI	TEST_PT	2.54 Red TEST_POINT	Generic	−
TP8	DET	TEST_PT	2.54 Red TEST_POINT	Generic	−
TP9	CRD_IO	TEST_PT	2.54 Red TEST_POINT	Generic	−
TP10	RST	TEST_PT	2.54 Red TEST_POINT	Generic	−
TP11	CLK	TEST_PT	2.54 Red TEST_POINT	Generic	−
TP12	C4	TEST_PT	2.54 Red TEST_POINT	Generic	−
TP13	C8	TEST_PT	2.54 Red TEST_POINT	Generic	−
TP14	CRD_VCC	TEST_PT	2.54 Red TEST_POINT	Generic	−
TP15	GND	TEST_PT	2.54 Black TEST_POINT	Generic	−

Banana plug 4 mm (red)
Banana plug 4 mm (black)
Plug power 2.5 mm/1 A
Power cable 2×0.5 mm^2 black 1 Meter

References

ISO/IEC 7816−3 International Standard, revision.
ISO/IEC 7816−4 International Standard, revision.
GSM11.11, version 7.3.0 – 1998, ETSI.
EMV Terminal Specifications For Payment Systems, Europay MasterCard Visa.
NCN6001 qualified data sheet, ON Semiconductor.

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